

Application No.: 10/675,039  
Reply to Final Rejection of January 13, 2005

### REMARKS/ARGUMENTS

Applicant requests the Examiner to more clearly identify the Information Disclosure Statement referred to in the communication mailed February 8, 2005. That communications indicated that an electronic IDS was filed October 5th. An electronic IDS was filed October 25, 2005. Further, the applicant did not receive a signed 1449 as indicated in that communication.

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

### Request for Interview

Applicant requests an oral interview with the Examiner prior to the Examiners issuing any rejection of the claims in the patent application.

### Summary of Invention

As set forth on page 8, beginning at line 14 through line 22: Referring now to FIG. 2, a data storage system 100 is shown for transferring data between a host computer/server 120 and a bank of disk drives 140 through a system interface 160. The system interface 160 includes: a plurality of, here 32 front-end directors 180<sub>1</sub>-180<sub>32</sub> coupled to the host computer/server 120; a plurality of back-end directors 200<sub>1</sub>-200<sub>32</sub> coupled to the bank of disk drives 140; a data transfer section 240, having a global cache memory 220, coupled to the plurality of front-end directors 180<sub>1</sub>-180<sub>16</sub> and the back-end directors 200<sub>1</sub>-200<sub>16</sub>; a messaging network 260, operative independently of the data transfer section 240, coupled to the plurality of front-end directors 180<sub>1</sub>-180<sub>32</sub> and the plurality of back-end directors 200<sub>1</sub>-200<sub>32</sub>, as shown; and, a cache memory manager 265.

As pointed out on page 9, line 19 through page 10, line 6: The cache memory manager 265 includes therein a memory 267 for storing a map maintaining a relationship between data stored in the cache memory 220 and data stored in the bank of disk drives 240.

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The cache memory manager 265 also includes a CPU coupled to the message network 260 and a memory controller 270 coupled between the CPU 268 and the memory 267, as shown. Further detail of the cache memory manager 265 and the message network 260 are provided herein in connection with FIG. 6. Suffice it to say here, however, that the cache memory manager 265 provides an interface between the host computer 102, the bank of disk drives 104, and the cache memory 220 via the message network 260 for determining for the front end directors 180<sub>1</sub>-180<sub>32</sub> and back-end directors 200<sub>1</sub>-200<sub>32</sub> whether data to be read from the bank of disk drives 104, or data to be written to the bank of disk drives 104, resides in the cache memory 220. The memory controller 270 contains hardware to assist in the management functions, including Content Addressable functions, to search the lists; and Indirect Addressing capability, to work linked lists and queues.

With such cache memory manager 265, the cache memory 220 in the data transfer section is not burdened with the task of transferring the director messaging but rather a messaging network is provided, operative independent of the data transfer section, for such messaging thereby increasing the operating bandwidth of the system interface. Further, the cache memory 220 is no longer burdened with the task of evaluating whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory.

As pointed out on page 18, lines 5 through line 9: The front-end and back-end directors 18<sub>1</sub>-18<sub>4</sub>, 20<sub>1</sub>-20<sub>4</sub> and the global cache memory communicate with one another through a packet switching network. The packet switching network includes crossbar switches 32 coupled to each one the directors, as shown, and a packet switching network section 26. The cache memory manager 265 is interconnected to the packet switching network via the packet switching network section 26.

#### Grounds of Rejection to be Reviewed

Whether claims 1-6 are unpatentable under 35 U. S. C. 103 as being obvious over Dobecki (U. S. Patent No. 6,611,879 in view of Armilli et al. (Published U. S. Patent Application 2003/0009643)).

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Argument:

Claim 1 points out that the system includes:

a cache memory manager, adapted to receive queries from the plurality of directors, such cache memory manager having therein a memory for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives;

wherein the cache memory manager receives the queries from the plurality of directors and operates independently of the plurality of directors in processing such queries to determine for the querying directors whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory; (emphasis added)

It is respectfully submitted that Arimilli et al., do not have a cache memory manager, adapted to receive queries from the plurality of directors, such cache memory manager having therein a memory for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives wherein the cache memory manager receives the queries from the plurality of directors and operates independently of the plurality of directors in processing such queries to determine for the querying directors whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory, as set forth in claim 1.

Further, claim 1 points out the system includes a packet switching network and that the system includes that four elements (i.e., (1) the cache memory manager; (2) the plurality of front end directors; (3) the plurality of back end directors; and (4) the cache memory) interconnected through the packet switching network. With Dobecki, all four elements set forth above are not connected to the common packet switching network. Thus claim 1 points out that the cache memory manager, plurality of front end directors, plurality of back end directors and cache memory are interconnected through the packet switching network. Such arrangement is not described or suggested in Dobecki or Arimilli et al. (Published U. S. Patent Application 2003/0009643).

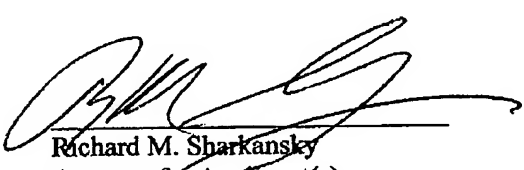
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In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 05-0889 for the cost of such extension.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

Respectfully submitted,

6-10-2005  
Date

  
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